Amendments to the Claims:

1-15. (Cancelled)

16. (Currently Amended) A semiconductor package, comprising:

a leadframe having:

a chip paddle defining opposed top and bottom surfaces and a plurality of sides and corners; and

at least two sets of leads extending along respective ones of the sides of the chip paddle in spaced relation thereto, each set of leads including at least two outer leads and at least one inner lead disposed between the outer leads, the inner and outer leads of each set each defining opposed top and bottom surfaces, with at least portions of the bottom surfaces of the outer leads of each set each being of a first length and at least a portion of the bottom surface of the inner lead of each set being of a second length which is unequal to the first length;

a semiconductor chip mounted to the top surface of the chip paddle and electrically connected to at least one of the inner and outer leads; and

an encapsulation material covering the leadframe and the semiconductor chip such that the portions of the bottom surfaces of the inner and outer leads of each set which are of the second length and the first length, respectively, are completely exposed in the encapsulation material and **are** arranged to intersect a single straight line extending between the outer leads.

17. (Previously Presented) The semiconductor package of Claim 16 comprising multiple sets of leads which extend along respective ones of each of the sides of the chip paddle in spaced relation thereto.

18. (Cancelled)

19. (Previously Presented) The semiconductor package of Claim 16 wherein the first length of the exposed portion of the bottom surface of each of the outer leads exceeds the second length of the exposed portion of the bottom surface of the inner lead.

20. (Previously Presented) The semiconductor package of Claim 16 wherein the first length of the exposed portion of the bottom surface of each of the outer leads is less than the second length of the exposed portion of the bottom surface of the inner lead.

21. (Previously Presented) The semiconductor package of Claim 16 wherein at least a portion of the bottom surface of the chip paddle is exposed in the encapsulation material.

22. (Previously Presented) The semiconductor package of Claim 21 wherein:

the encapsulation material defines a generally planar bottom surface;

the exposed portion of the bottom surface of the chip paddle is generally planar and substantially flush with the bottom surface of the encapsulation material; and

the exposed portions of the bottom surfaces of the inner and outer leads are each generally planar and substantially flush with the bottom surface of the encapsulation material.

23. (Previously Presented) The semiconductor package of Claim 16 wherein the leadframe further comprises at least one tie bar attached to and extending from at least one of the corners of the chip paddle, the tie bar defining opposed top and bottom surfaces.

24. (Previously Presented) The semiconductor package of Claim 23 wherein at least a portion of the bottom surface of the at least one tie bar is exposed in the encapsulation material.

25. (Previously Presented) A semiconductor package comprising:

a semiconductor chip defining multiple sides;

at least two sets of leads extending along respective ones of the sides of the semiconductor chip in spaced relation thereto, each set of leads including at least two outer leads and at least one inner lead disposed between the outer leads, the inner and outer leads of each set each defining opposed top and bottom surfaces, with at least portions of the bottom surfaces of the outer leads of each set each being of a first length and at least a portion of the bottom surface of the inner lead of each set being of a second length which is unequal to the first length, the semiconductor chip being electrically connected to at least one of the inner and outer leads; and

an encapsulation material defining a bottom surface which includes a peripheral edge, the encapsulation material covering the inner lead, the outer leads and the semiconductor chip such that the portions of the bottom surfaces of the inner and outer leads of each set which are of the second length and the first length, respectively, are completely exposed in the encapsulation material and extend to the peripheral edge of the bottom surface.

26. (Previously Presented) The semiconductor package of Claim 25 comprising multiple sets of leads which extend along respective ones of each of the sides of the semiconductor chip.

27. (Cancelled)

28. (Previously Presented) The semiconductor package of Claim 25 wherein the first length of the exposed portion of the bottom surface of each of the outer leads exceeds the second length of the exposed portion of the bottom surface of the inner lead.

29. (Previously Presented) The semiconductor package of Claim 25 wherein the first length of the exposed portion of the bottom surface of each of the outer leads is less than the second length of the exposed portion of the bottom surface of the inner lead.

30. (Previously Presented) The semiconductor package of Claim 25 wherein:

the encapsulation material defines a generally planar bottom surface; and

the exposed portions of the bottom surfaces of the inner and outer leads are each generally planar and substantially flush with the bottom surface of the encapsulation material.

31. (Previously Presented) In a semiconductor package comprising a plurality of leads which each have a bottom surface including at least a portion which is completely exposed in an encapsulation material, and a semiconductor chip which defines multiple sides, is covered by the encapsulation material and electrically connected to at least one of the leads, the improvement comprising:

providing at least two sets of the leads which are extended along respective ones of the sides of the semiconductor chip and each include at least two outer leads and at least one inner lead disposed between the outer leads, with the portion of the bottom surface of each of the outer leads of each set which is completely exposed in the encapsulation material being of a first length, the portion of the bottom surface of the inner lead of each set which is completely exposed in the encapsulation material being of a second length which is unequal to the first length, and the exposed portions of the bottom surfaces of the inner and outer leads of each set being arranged to intersect a single straight line extending between the outer leads.

32. (Previously Presented) The semiconductor package of Claim 31 wherein multiple sets of the extended along respective ones of each of the sides of the semiconductor chip.

33. (Cancelled)

34. (Previously Presented) The semiconductor package of Claim 31 wherein the first length of the exposed portion of the bottom surface of each of the outer leads exceeds the second length of the exposed portion of the bottom surface of the inner lead.

35. (Previously Presented) The semiconductor package of Claim 31 wherein the first length of the exposed portion of the bottom surface of each of the outer leads is less than the second length of the exposed portion of the bottom surface of the inner lead.

36. (Previously Presented) The semiconductor package of Claim 16, wherein:

the encapsulation material defines a bottom surface which includes a peripheral edge; and

the exposed portions of the bottom surfaces of the outer and inner leads of each set extend to the peripheral edge of the bottom surface.

37. (Previously Presented) The semiconductor package of Claim 31, wherein:

the encapsulation material defines a bottom surface which includes a peripheral edge; and

the exposed portions of the bottom surfaces of outer and inner leads of each set extend to the peripheral edge of the bottom surface.